SEMICONDUCTORS

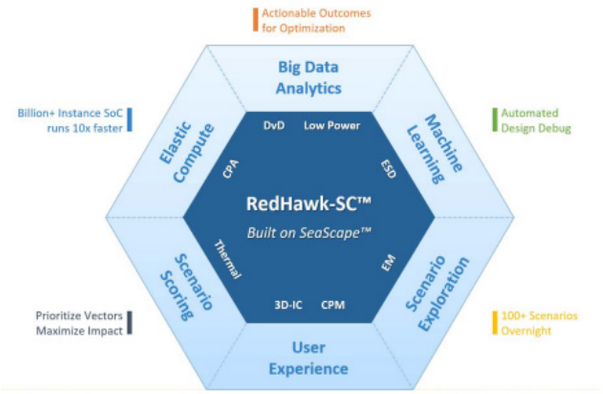
Ansys PathFinder-SC

Next-Generation SoC ESD Integrity Analysis

Ansys PathFinder-SC™ is the next-generation SoC power noise signoff platform designed to enable sub-16nm design success. PathFinder-SC provides a high-capacity solution for verifying the protective circuitry found on all chips that protect them from electrostatic discharge (ESD) and damage from voltage spikes. This technology has become increasingly pivotal as silicon technology continues to shrink to 3nm and below, where these tiny transistors need to be protected by critical ESD circuitry that is checked, verified, and signed off with PathFinder-SC. PathFinder-SC is built on Ansys SeaScape™, the world's first custom-designed big data platform for electronic system design and simulation. SeaScape provides per-core scalability, flexible design data access, instantaneous design bring-up, MapReduce-enabled analytics and many other revolutionary capabilities. SeaScape technology allows PathFinder-SC to deliver over 5x faster turnaround for ultra-large SoCs, which makes it ideal for today's large, high-speed semiconductor designs in artificial intelligence, imaging, networking, and 5G and 6G telecommunications.

Importance of ESD Integrity Analysis and Market Failure Trend

Industry surveys indicate that up to 35 percent of integrated circuit (IC) field failures are related to ESD. Advanced process technologies, higher operating frequencies, increased analog-digital integration, and smaller product footprints only exacerbate the problem.



RedHawk-SC Platform

Elastic Compute Scalability

PathFinder-SC shares core engines from next-generation SoC power noise signoff platform, Ansys RedHawk-SC™. With unparalleled scalability across thousands of cores using big data techniques, PathFinder-SC performs ESD Integrity Analysis on billion+ instance SoC designs with extremely fast turnaround time on commodity hardware. PathFinder-SC runs the largest designs, using low memory cores, even if they reside on different machines. PathFinder-SC starts working as soon as a single core is available. It proportionately speeds up as more cores become available and has the resiliency to recover should any core or machine become unresponsive. Because PathFinder-SC can utilize unused cores, it increases utilization rates of compute farms, thereby decreasing overall hardware costs. Unlike other tools, it does not require dedicated hardware, even for the largest designs. This elastic scalability is what enables PathFinder-SC to process designs of unprecedented size with flat accuracy, high resolution extracted networks, and multiple scenarios.

Big Data Analytics

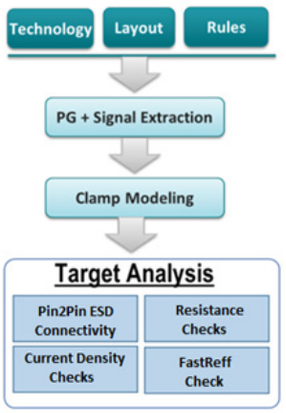
Big data analytics enable rapid data mining and analytics to drive actionable outcomes and optimization. Using custom data analytics, you can identify and prioritize only those design fixes that are key to product success. Custom analytics powered by MapReduce enable you to query the largest designs in minutes.

Multi-site Collaboration Using Thin Client Support

PathFinder-SC is built for multi-site collaboration and effective design analysis. Users across multiple sites can simultaneously view, debug, and explore design and simulation results. You can bring up the largest designs in small memory machines in minutes and simultaneously view and optimize the same database across multiple sites.

Comprehensive ESD Coverage: HBM and CDM

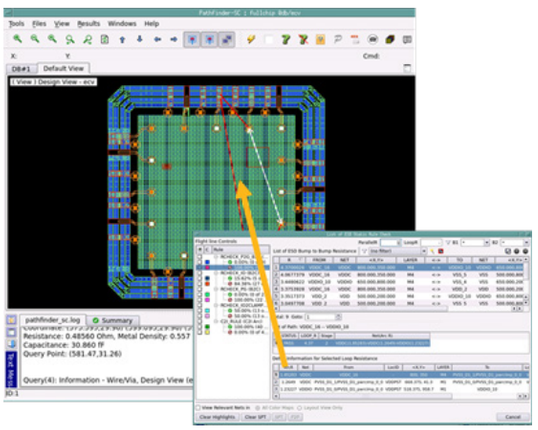
PathFinder-SC is designed to simulate human body model (HBM) and charge device model (CDM) events to ensure integrity of ICs with respect to ESD. With its comprehensive connectivity, resistance, and interconnect failure analysis, it practically covers every wire segment/via in the ESD discharge path.



PathFinder-SC ESD Analysis Flow

Fast Debug with Powerful GUI and Clamp Modeling

PathFinder-SC features layout-based ESD analysis with integrated clamp modeling, extraction, and simulation engines, as well as a versatile graphical user interface (GUI) for result analysis and debugging. Along with several detailed reporting mechanisms, GUI provides visibility into ESD bus robustness as well as victim devices that may be impacted during ESD discharge.



PathFinder-SC layout-based analysis and root cause detection

Accuracy

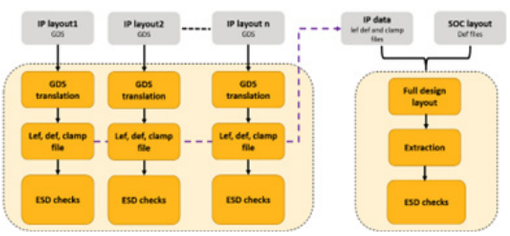
PathFinder-SC is built on top of foundry-certified and silicon-proven RedHawk-SC engines, which demonstrate good correlation with PathFinder.

Full-chip Capacity

PathFinder-SC can achieve over 5x speed-up on large GDS processing and full-chip ESD analysis utilizing elastic compute with commodity hardware and cloud.

Comprehensive Coverage from Cell-level to Full-chip

PathFinder-SC can be used at the ESD cell level or the IO/IP level, all the way to full-chip integration to provide comprehensive ESD coverage. It will also be able to create chip-level ESD models for system-level ESD analysis.



IP and SoC design handling in PathFinder-SC

Advanced Usage Models

PathFinder-SC can perform full-chip CDM checks (driver-receiver, clamp to instance, etc.) and provide customizable applications, such as grid continuity checks.

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